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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,534	09/25/2001	Katsushi Nagaba	81790.0219	3774

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EXAMINER
ABRAHAM, FETSUM

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/965,534	Applicant(s) NAGABA ET AL.
	Examiner Fetsum Abraham	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *11-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claims rejection

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens (6,173,345).

As for claims 1, 5,7 the patent discloses an integrated circuit in fig 2 comprising a delay register circuit (249) which received data from the serial control logic circuit (248) (see column 5, 35-45), a variable delay circuit (244) receiving the output of the register, and a driver (242) receiving the output of the delay circuit. Although the application of clock signals in the circuit is not presented in detail conforming to the claim language, it is clear that all data transfers in logic circuits, delay signals and register read/write functions are performed by clock signals. The controller (205) would not perform its controlling duties of data management without control clock signals. Therefore, it would have been obvious to one skilled in the art to safely conclude that the claimed structure is fully represented by the patent, since clock signals in write/read oriented circuits are inherent to the circuits.

As for claim 7 specifically, element (245) can be perceived as the first delay adjustment circuit that receives the first delay signal from delay block (249) and the first driver at the same

time since it is in electrical contact with the delay circuit. Like wise, the driver (242) as a second delay adjustment circuit from the over all delay circuit (244).

As for claims 2-4,6,8,9, forming drivers off chip does not alter the valid application of the patent since all elements in the structure can be formed in separate chips at the expense of elongated processing steps and additional materials. As for said read data signal, an input to any register that can be stored in the register is read/written data by the register. Further more, drivers are known buffer circuits in the art since they can hold data for predetermined time. Please note that registers are also memory elements with full capacity of storing data, which is a typical performance by all buffer circuits (see column 5, 30-45).

Further, as for claims 4,10, the contents of ID circuits (247) are address signals which are also transferred to the driver circuit via the delay circuit (see column 5, 42-50).

Claims 11-13 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Examiner's response to applicant's argument

The applicant argues that the prior art omits to teach outputting a delay adjustment signal and drivers receiving the delay adjustment signals. This argument has been considered but found moot in view of the reference at hand. The examination of the claimed performance of the claimed circuit was based on the fact that any circuit receiving a delay signal is expected to adjust to the signal since it is driven by it. This basic performance indicated that there is an inherent adjustment process going on between two circuits associated with delay signals. In light of this basic understanding of circuits in general, the applied reference has been appropriate.

Any inquiry concerning this communication should be directed to Fetsum Abraham at telephone number (703) 305,3793, or by E-mail at ***fetsum.abraham@uspto.gov.***

Any inquiry of a general nature or relating to the status of this application should be directed to the ***SPE of AU***:2826 at (703)308-6601, or the ***Group receptionist*** at (703) 308-0956.

Fetsum Abraham/4/1/03